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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,261	12/02/2003	Ping Hsu	NTCP0018USA	1260

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EXAMINER	
KENNEDY, JENNIFER M	
ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,261	HSU, PING	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 1 is objected to because of the following informalities: In lines 24-25, the claim recites "a top surface of said second polysilicon layer and said exposed substrate define a second recess" the examiner suggests amending to state --wherein a top surface of said second polysilicon layer and said exposed substrate define a second recess-- so as to make the phrase more clear. Appropriate correction is required.

Claim 1 is objected to because of the following informalities: In line 32, the examiner suggests replacing "spacer on sidewall" with –spacer on the sidewall—for grammatical correctness. Appropriate correction is required.

Claim 8 is objected to because of the following informalities: In lines 23-25, the claim recites "a top surface of said second polysilicon layer and said exposed substrate define a second recess" the examiner suggests amending to state --wherein a top surface of said second polysilicon layer and said exposed substrate define a second recess-- so as to make the phrase more clear. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 8 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Wu (U.S. Patent No. 6,552,382).

Wu discloses a method for fabricating a trench capacitor, comprising: providing a substrate (300) having thereon a pad oxide layer (301) and a pad nitride layer (305);

etching in order of said pad nitride layer, said pad oxide layer, and said substrate to form a deep trench (see Figure 3D-3E);

doping said deep trench to form a buried diffusion plate in said substrate at a lower portion of said deep trench (see column 6, lines 30-55);

lining said deep trench with a node dielectric layer (311);

performing a first polysilicon deposition (312) and recess etching to embed a first polysilicon layer on said node dielectric layer at said lower portion of said deep trench, and said first polysilicon layer having a top surface, wherein said top surface of said first polysilicon layer and sidewall of said deep trench define a first recess (see column 6, line 60 through column 7, line 5 and Figure 3E);

forming a collar oxide layer (313) on sidewall of said first recess;

performing a second polysilicon deposition (314) and recess etching to embed a second polysilicon layer on said first polysilicon layer (see column 7, lines 15-25);

removing said collar oxide layer that is not covered by said second polysilicon layer to expose said substrate at an upper portion of said deep trench, and a top surface of said second polysilicon layer and said exposed substrate to define a second recess (see column 7, lines 25-40);

forming a single-sided spacer on sidewall of said second recess (see column 8, lines 13-16, and Figure 3H); and

performing a third polysilicon deposition and recess etching to embed a third polysilicon layer on said second polysilicon layer and said collar oxide layer (see column 8, lines 15-30).

In re claim 10, Wu disclose the method wherein said single-sided spacer is used to isolate a portion of said third polysilicon layer from said substrate (see Figure 3H).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (U.S. Patent No. 6,368,912) in view of Wu (U.S. Patent No. 6,552,382) and Manley et al. (U.S. Patent No. 6,221,735).

Chang et al. disclose a method for fabricating a trench capacitor, comprising:

providing a substrate (100) having thereon a pad oxide layer (105) and a pad nitride layer (120);

etching in order of said pad nitride layer, said pad oxide layer, and said substrate to form a deep trench (see column 2, line 64 through column 3, line 3);

doping said deep trench to form a buried diffusion plate (130) in said substrate at a lower portion of said deep trench;

lining said deep trench with a node dielectric layer (135);

performing a first polysilicon deposition (140) to embed a first polysilicon layer on said node dielectric layer at said lower portion of said deep trench, and said first polysilicon layer having a top surface, wherein said top surface and sidewall of said deep of said first polysilicon layer trench define a first recess;

forming a collar oxide layer (145) on sidewall of said first recess;

performing a second polysilicon (150) deposition to embed a second polysilicon layer on said first polysilicon layer;

removing said collar oxide layer that is not covered by said second polysilicon layer (see Figure 1A) to expose said substrate at an upper portion of said deep trench, and a top surface of said second polysilicon layer and said exposed substrate define a second recess;

filling said second recess with a spacer material layer (175);

forming a masking layer (182) on said spacer material layer, and said masking layer masking a portion of said spacer material layer;

anisotropically etching said spacer material layer not covered by said masking layer, to form a single-sided spacer on sidewall of said second recess (see column 4,lines 18-30); and

performing a third polysilicon deposition (181) to embed a third polysilicon layer on said second polysilicon layer and said collar oxide layer.

Chang et al. do not disclose the method wherein the polysilicon layers are recessed etched. Wu et al. discloses the method of recess etching the polysilicon layers (see column 6, line 65 through column 7, line 5, column 7, lines 15-20, and column 8, lines 15-22). It would have been obvious to one of ordinary skill in the art at the time the invention was made to embed the polysilicon layers by a deposition process and then a subsequent recess etching so as to form the required vertical level of polysilicon for the capacitor plate coupled to the dielectric node and buried plate, the polysilicon for the connecting portion coupled to the collar oxide and the polysilicon for the gate coupled to the gate oxide, respectively, which allows for an operable device without short circuiting.

The combined Chang et al. and Wu disclose the method of utilizing a nitride layer as a mask to etch the spacer material (see Chang et al. 182), but neither Chang et al. nor Wu disclose the method of utilizing photoresist for masking. Manley et al. disclose the use of photoresist or nitride when making to form a trench (see column 4, lines 55-60 and column 3, lines 55-60). It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize photoresist instead of nitride in the method of the combined Chang et al. and Wu, because as Manley et al. teaches

photoresist is a suitable material for masking and can be used interchangeably with nitride when masking and etching trenches and since it has been held to be within the general skill of the worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

In re claim 2, neither Chang et al. nor Wu disclose the method wherein said substrate is a silicon substrate. Manley et al. teaches utilizing a silicon substrate as a semiconductor substrate (see column 3, lines 42-45). It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a silicon substrate as the semiconductor substrate of the method of the combined Chang et al. and Wu because it is known that silicon has a large bandgap that results in smaller leakage currents and thereby allows silicon devices to be built with maximum operating temperature of about 150 degrees Celsius, and further it has been held to be within the general skill of the worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

In re claim 3, the combined Chang et al., Wu and Manley disclose the method of forming a shallow trench having a depth of 1.5 microns (see Wu column 4, line 65 through column 5, line 2). It is clear to the examiner that a "deep trench" of Wu would be deeper than 1.5 microns. However, neither Chang et al. nor Wu nor Manley et al. explicitly disclose the method wherein said deep trench has a depth that is larger than 6 microns below a surface of said substrate.

The examiner notes that Applicant does not teach that the particular depth solves any stated problem or are for any particular purpose. Therefore, the depth lacks criticality in the claimed invention and does not produce unexpected or novel results. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the deep trench at any depth greater than 6 microns since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

In re claim 4, Chang et al. does not disclose the method of doping the substrate to form the buried plate. Wu discloses the method wherein doping said deep trench to form a buried diffusion plate in said substrate involves the use of an arsenic silicate glass (ASG) film (see column 6, lines 34-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the method of forming the buried plate with ASG because it allows for a controlled doping.

In re claim 5, Chang et al. disclose the method wherein said node dielectric is a composite of silicon nitride and silicon oxide, but does not specifically state that the dielectric layer is an oxide-nitride-oxide (ONO) dielectric layer. Wu discloses the method of forming an ONO layer (see column 6, lines 58-60) as a composite dielectric layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the ONO layer as the composite dielectric layer Chang et al. because as Wu discloses it is a preferred dielectric for trench capacitors which allows for a thin dielectric with a sufficient dielectric constant.

In re claim 6, Chang et al. disclose the method wherein said spacer material layer is a thermal oxide, but does not explicitly disclose a silicon dioxide. The combined Chang et al., Wu and Manley et al. would necessarily have a silicon dioxide spacer material if the silicon substrate of Manley et al. were to be thermally oxidized. Further, it is noted that Wu discloses the method of forming other spacers of a silicon oxide layer (see column 4, lines 40-45). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the single-sided spacer of silicon oxide since Wu teaches that silicon oxide is a suitable material layer for a spacer that allows for isolation and further it has been held to be within the general skill of the worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

In re claim 7, Chang et al. disclose the method wherein said silicon dioxide is formed by thermal oxidation, but do not disclose wherein the silicon oxide is formed by chemical vapor deposition (CVD) method. Chang et al. disclose the method of forming another silicon oxide layer by HPCVD, a CVD method (see column 3, lines 24-37). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the silicon oxide layer of the spacer by a CVD method because as Chang et al. teaches an oxide may be made by a HPCVD method to allow for good step coverage.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (U.S. Patent No. 6,552,382).

Wu disclose the method as claimed and rejected above, including the method of forming the single-sided spacer of an oxide by a thermal oxidation process, but does not disclose the method wherein the single-sided spacer is made of silicon dioxide.

Wu discloses the method of forming other spacers of a silicon oxide layer (see column 4, lines 40-45). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the single-sided spacer of silicon oxide since Wu teaches that silicon oxide is a suitable material layer for a spacer that allows for isolation and further it has been held to be within the general skill of the worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Kennedy
Patent Examiner
Art Unit 2812

jmk